UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., **Plaintiff,** **v.** **MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,** **Defendants.**	**Civil Action No. 2:22-CV-203-JRG-RSP**

DEFENDANTS' ANSWER, AFFIRMATIVE DEFENSES, AND COUNTERCLAIMS TO PLAINTIFF'S COMPLAINT

Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC ("Micron" or "Defendants") submit this Answer, Affirmative Defenses, and Counterclaims in response to Plaintiff Netlist, Inc.'s ("Netlist" or "Plaintiff") Complaint.

The numbered paragraphs below correspond to the numbered paragraphs in the Complaint and constitute Defendants' responsive admissions, denials, and allegations thereto. Except as Defendants otherwise admit expressly below, Defendants deny each and every allegation contained in the Complaint, including, without limitation, the headings, subheadings, footnotes, diagrams, and tables contained in the Complaint.

Defendants reserve the right to amend or supplement their Answer and Affirmative Defenses.

ANSWER TO COMPLAINT

1. Micron admits that Plaintiff's pleading purports to be a Complaint against Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron

Technology Texas, LLC. Micron lacks sufficient knowledge or information to form a belief as to the truth of the other allegations in paragraph 1 of the Complaint and therefore denies the same.

2. Micron admits that purported copies of U.S. Patent Nos. 10,860,506 (the "'506 Patent"), 10,949,339 (the "'339 Patent"), 11,016,918 (the "'918 Patent"), 11,232,054 (the "'054 Patent"), 8,787,060 (the "'060 Patent"), and 9,318,160 (the "'160 Patent") (collectively, the "Asserted Patents") are attached to the Complaint as Exhibits 1 through 6, respectively. Micron lacks sufficient knowledge or information to form a belief as to the truth of the other allegations in paragraph 2 of the Complaint and therefore denies the same.

THE PARTIES

3. Micron lacks sufficient knowledge or information to form a belief as to the truth of the allegations in paragraph 3 of the Complaint and therefore denies the same.

4. Micron admits that it makes memory products in semiconductor fabrication plants for sale to customers. Except as expressly admitted, Micron denies the remaining allegations in paragraph 4.

5. Micron Technology, Inc. ("MTI") admits that it is a Delaware corporation. MTI admits that it leases a property located at 950 W. Bethany Drive, Suite 120, Allen, Texas 75013. MTI admits that it is registered to do business in Texas. MTI admits that it can be served with certain process through its registered agent for service of process, Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218. Except as expressly admitted, Micron denies the remaining allegations in paragraph 5.

6. Micron Semiconductor Products, Inc. ("MSP") admits that it is an Idaho corporation. MSP admits that it is registered to do business in Texas. MSP admits that it can be served with certain process through its registered agent for service of process, Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218. Except as expressly admitted,

Micron denies the remaining allegations in paragraph 6.

7. Micron Technology Texas, LLC ("Micron Texas") admits that it is an Idaho limited liability company. Micron Texas admits that it uses the property located at 950 West Bethany Drive, Suite 120, Allen, Texas 75013-3837. Micron Texas admits that it can be served with certain process through its registered agent for service of process, Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218. Except as expressly admitted, Micron denies the remaining allegations in paragraph 7 of the Complaint.

8. Micron admits that MSP and Micron Texas are wholly owned subsidiaries of MTI. Micron admits that MTI currently does not separately report revenue from MSP or Micron Texas in its public filings submitted to the Securities Exchange Commission. Except as expressly admitted, Micron denies the remaining allegations in paragraph 8.

9. Micron admits that it makes memory products in semiconductor fabrication plants for sale to customers. Except as expressly admitted, Micron denies the remaining allegations in paragraph 9.

10. Micron denies the allegations of paragraph 10.

JURISDICTION AND VENUE

11. Paragraph 11 contains conclusions of law and not averments of fact to which the rules require an answer, but insofar the rules require an answer, Micron admits that the Complaint purports to assert an action under the patent laws of the United States, 35 U.S.C. § 271 *et seq*., and that this Court has subject matter jurisdiction over actions for patent infringement under 28 U.S.C. § 1338(a).

12. Based solely on the allegations in the Complaint, and assuming (without admitting) them to be true, Micron does not contest personal jurisdiction in this district in this case. Except as expressly admitted, Micron denies the remaining allegations in paragraph 12.

13. Based solely on the allegations in the Complaint, and assuming (without admitting) them to be true, Micron does not contest personal jurisdiction in this district in this case. Except as expressly admitted, Micron denies the remaining allegations in paragraph 13.

14. Micron denies the allegations of paragraph 14.

FACTUAL ALLEGATIONS

Background

15. Micron lacks sufficient knowledge or information to form a belief as to the truth of the allegations in paragraph 15 of the Complaint and therefore denies the same.

16. Micron lacks sufficient knowledge or information to form a belief as to the truth of the allegations in paragraph 16 of the Complaint and therefore denies the same.

17. Micron denies that the allegations in paragraph 17 of the Complaint are complete or accurate, and on that basis denies them.

18. Micron admits that the JEDEC Solid State Technology Association ("JEDEC") is a standardization body that develops open standards and publications for a broad range of semiconductor technologies, including memory modules. Micron denies that the remaining allegations in paragraph 18 of the Complaint are complete or accurate, and on that basis denies them.

19. Micron admits that HBM is a type of memory technology. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the image shown in paragraph 19 (pg. 6) of the Complaint. Micron admits that a purported copy of a Micron White Paper titled "The Demand for High-Performance Memory" is attached to the Complaint as Exhibit 11 and includes the image shown in paragraph 19 (pg. 7) of the Complaint. Micron denies that the remaining allegations in paragraph 19 of the Complaint are complete or accurate, and on that basis denies them.

The Asserted Netlist Patents

The '506 Patent

20. Micron admits that the '506 Patent states, on its face, that it is titled "Memory Module With Timing-Controlled Data Buffering" and that it lists Hyun Lee and Jayesh R. Bhakta as inventors. Micron further admits that the '506 Patent states, on its face, that it was filed as Application No. 16/391,151 on April 22, 2019, issued as a patent on December 8, 2020, and purports to claim priority to, among others, a utility application filed on July 27, 2013 (No. 13/952,599) and a provisional application filed on July 27, 2012 (No. 61/676,883). Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 20 of the Complaint, and therefore denies them.

21. Micron admits that Netlist alleged infringement of the '506 Patent in the Complaint. Micron denies the remaining allegations in paragraph 21 of the Complaint.

22. Micron admits that the '506 Patent includes the language "distribution of control signals and a control clock signal in the memory module is subject to strict constraints." '506 Patent at 2:17-19. Micron admits that the '506 Patent includes the language "control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules." '506 Patent at 2:19-23. Micron admits that the '506 Patent includes the language "[t]he balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections." '506 Patent at 2:23-26. Micron admits that the '506 Patent includes the language "such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules." '506 Patent at 2:32-34. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 22 of the

Complaint, and therefore denies them.

23. Micron admits that the '506 Patent includes the language "[e]ach respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals." '506 Patent at Abstract. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 23 of the Complaint, and therefore denies them.

24. Micron admits that the '506 Patent includes Figure 2A (modified in paragraph 24 of the Complaint with Netlist annotations). Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 24 of the Complaint, and therefore denies them.

25. Micron admits that the '506 Patent includes the language "[b]ecause the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-(n−1) in the exemplary configuration shown in FIG. 2." '506 Patent at 9:52-59. Micron admits that the '506 Patent includes the language "each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent

read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100 . . .” ’506 Patent at 10:11-20. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in Paragraph 25 of the Complaint, and therefore denies them.

The ’339 Patent

26. Micron admits that the ’339 Patent states, on its face, that it is titled “Memory Module With Controlled Byte-Wise Buffers” and that it lists Hyun Lee and Jayesh R. Bhakta as inventors. Micron further admits that the ’339 Patent states, on its face, that it was filed as Application No. 15/470,856 on March 27, 2017, issued as a patent on March 16, 2021, and purports to claim priority to U.S. Patent Application No. 12/504,131 filed on July 16, 2009, U.S. Patent Application No. 12/761,179 filed on April 15, 2010, and U.S. Application No. 13/970,606 filed on August 20, 2013. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in Paragraph 26 of the Complaint, and therefore denies them.

27. Micron admits that Netlist alleged infringement of the ’339 Patent in the Complaint. Micron denies the remaining allegations in paragraph 27 of the Complaint.

28. Micron admits that the ’339 Patent includes the language “consideration is always given to memory density, power dissipation (or thermal dissipation), speed, and cost.” ’339 Patent at 2:5-7. Micron admits that the ’339 Patent includes the language “[g]enerally, these attributes are not orthogonal to each other, meaning that optimizing one attribute may detrimentally affect another attribute. For example, increasing memory density typically causes higher power dissipation, slower operational speed, and higher costs.” ’339 Patent at 2:7-12. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 28 of the Complaint, and therefore denies them.

29. Micron admits that the ’339 Patent includes the language “[t]he registered address

and control signals selects one of the multiple ranks to perform the read or write operation. The module controller further outputs a set of module control signals in response to the input address and control signals. The memory module further comprises a plurality of byte-wise buffers controlled by the set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank." '339 Patent at Abstract. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 29 of the Complaint, and therefore denies them.

30. Micron admits that the '339 Patent includes Figure 3A (modified in paragraph 30 of the Complaint with Netlist annotations). Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 30 of the Complaint, and therefore denies them.

31. Micron admits that the '339 Patent includes the language "[r]eferring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. . . . Thus, the memory controller 420, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system . . ." '339 Patent at 17:14-42. Micron admits that the '339 Patent includes the language

"the data transmission circuit 416 comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more transmission circuits 416 has the same bit width as does the associated memory devices 412 per rank to which the data transmission circuit 416 is operatively coupled." '339 Patent at 13:31-36. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 31 of the Complaint, and therefore denies them.

The '918 Patent

32. Micron admits that the '918 Patent states, on its face, that it is titled "Flash-DRAM Hybrid Memory Module" and that it lists Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta as inventors. Micron further admits that the '918 Patent states, on its face, that it was filed as Application No. 17/138,766 on December 30, 2020, issued as a patent on May 25, 2021, and purports to claim priority to U.S. Application No. 15/934,416 filed on March 23, 2018, U.S. Application No. 14/840,865 filed on August 31, 2015, U.S. Application No. 14/489,269 filed on September 17, 2014, U.S. Application No. 13/559,476 filed on July 26, 2012, U.S. Application No. 12/240,916 filed on September 29, 2008, and U.S. Application No. 12/131,873 filed on June 2, 2008, as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871). Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 32 of the Complaint, and therefore denies them.

33. Micron admits that Netlist alleged infringement of the '918 Patent in the Complaint. Micron denies the remaining allegations in paragraph 33 of the Complaint.

34. Micron admits that the '918 Patent includes the language "[f]irst, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or

more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." '918 Patent at Abstract. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 34 of the Complaint, and therefore denies them.

35. Micron admits that the '918 Patent includes Figure 16. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 35 of the Complaint, and therefore denies them.

36. Micron admits that the '918 Patent includes the language "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller." '918 Patent at 28:3-15. Micron admits that the '918 Patent includes the language "[t]he conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters." '918 Patent at 29:18-19. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 36 of the Complaint, and therefore denies them.

37. Micron admits that the '918 Patent includes the language "the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger

condition, such as, for example, a power failure or power reduction or a request from the host system." '918 Patent at 24:12-16. Micron admits that the '918 Patent includes the language "the memory system 1010 detects that the system voltage is below a certain threshold voltage." '918 Patent at 24:24-25. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 37 of the Complaint, and therefore denies them.

38. Micron admits that the '054 Patent purports to be a continuation of the '918 Patent. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 38 of the Complaint, and therefore denies them.

39. Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 39 of the Complaint, and therefore denies them.

The '054 Patent

40. Micron admits that the '054 Patent states, on its face, that it is titled "Flash-DRAM Hybrid Memory Module" and that it lists Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta as inventors. Micron further admits that the '054 Patent states, on its face, that it was filed as Application No. 17/328,019 on May 24, 2021, issued as a patent on January 25, 2022, and purports to claim priority to U.S. Application No. 17/138,766 filed on December 30, 2020, U.S. Application No. 15/934,416 filed on March 23, 2018, U.S. Application No. 14/840,865 filed on August 31, 2015, U.S. Application No. 14/489,269 filed on September 17, 2014, U.S. Application No. 13/559,476 filed on July 26, 2012, U.S. Application No. 12/240,916 filed on September 29, 2008, and U.S. Application No. 12/131,873 filed on June 2, 2008, as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871). Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 40 of the Complaint, and therefore denies them.

41. Micron admits that Netlist alleged infringement of the '054 Patent in the Complaint.

Micron denies the remaining allegations in paragraph 41 of the Complaint.

42. Micron admits that the '054 Patent includes the language "[f]irst, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." '054 Patent at Abstract. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 42 of the Complaint, and therefore denies them.

43. Micron admits that the '054 Patent includes Figure 16. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 43 of the Complaint, and therefore denies them.

44. Micron denies the allegations of paragraph 44.

The '060 and '160 Patents

45. Micron admits that the '060 Patent states, on its face, that it is titled "Method and Apparatus for Optimizing Driver Load in a Memory Package" and that it lists Hyun Lee as the sole inventor. Micron further admits that the '060 Patent states, on its face, that it was filed as Application No. 13/288,850 on November 3, 2011, issued as a patent on July 22, 2014, and purports to claim priority to a provisional application filed on November 3, 2010 (U.S. Application No. 61/409,893). Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 45 of the Complaint, and therefore denies them.

46. Micron admits that the '160 Patent states, on its face, that it is a continuation of the '060 patent, that it is titled "Memory Package with Optimized Driver Load and Method of

Operation," and that it lists Hyun Lee as the sole inventor. Micron further admits that the '160 Patent states, on its face, that it was filed as Application No. 14/337,168 on July 21, 2014, issued as a patent on April 19, 2016, and purports to claim priority to U.S. Application No. 13/288,850 (which issued as the '060 Patent) and a provisional application filed on November 3, 2010 (U.S. Application No. 61/409,893). Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 46 of the Complaint, and therefore denies them.

47. Micron admits that Netlist alleged infringement of the '060 and '160 Patents in the Complaint. Micron denies the remaining allegations in paragraph 47 of the Complaint.

48. Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 48 of the Complaint, and therefore denies them.

49. Micron admits that the '060 and '160 Patents include the language "[t]he first die interconnect is in electrical communication with a data port of a first array die and a data port of a second array die and not in electrical communication with data ports of a third array die. The second die interconnect is in electrical communication with a data port of the third array die and not in electrical communication with data ports of the first array die and the second array die. The apparatus includes a control die that includes a first data conduit configured to transmit a data signal to the first die interconnect and not to the second die interconnect, and at least a second data conduit configured to transmit the data signal to the second die interconnect and not to the first die interconnect." '060 Patent at Abstract; '160 Patent at Abstract. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 49 of the Complaint, and therefore denies them.

50. Micron admits that the '060 and '160 Patents both include Figure 2 and that Figure 2 is identical in each patent. Micron lacks knowledge or information sufficient to form a belief as

to the truth of the other allegations in paragraph 50 of the Complaint, and therefore denies them.

51. Micron admits that the '060 and '160 Patents include the language "[e]ach of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320." '060 Patent at 5:54-62; '160 Patent at 5:57-65. Micron lacks knowledge or information sufficient to form a belief as to the truth of the other allegations in paragraph 51 of the Complaint, and therefore denies them.

Micron's Activities[1]

52. Micron admits that certain Micron entities design and manufacture memory and storage products, including DRAM, DIMMs, and Multichip Packages. Except as expressly admitted, Micron denies the remaining allegations of paragraph 52.

53. Micron admits that it received a letter from Netlist dated April 28, 2021. Except as expressly admitted, Micron denies the remaining allegations of paragraph 53.

DDR4 Memory Modules

54. Micron admits that the Complaint purports to define the "accused DDR4 products" as stated in paragraph 54. Except as expressly admitted, Micron denies the remaining allegations of paragraph 54.

DDR5 Memory Modules

55. Micron admits that the Complaint purports to define the "accused DDR5 products"

[1] Micron denies the allegation contained in the header preceding paragraph 52.

as stated in paragraph 55. Except as expressly admitted, Micron denies the remaining allegations of paragraph 55.

56. Micron admits that the Complaint purports to define the "accused DDR5 products" as stated in paragraph 56. Except as expressly admitted, Micron denies the remaining allegations of paragraph 56.

57. Micron admits that the Complaint purports to define the "accused DDR5 products" as stated in paragraph 57. Except as expressly admitted, Micron denies the remaining allegations of paragraph 57.

58. Micron admits that a purported copy of a Micron White Paper titled "Micron® DDR5: Client Module Features" is attached to the Complaint as Exhibit 10 and includes the image shown in paragraph 58 of the Complaint. Micron denies that the remaining allegations in paragraph 58 of the Complaint are complete or accurate, and on that basis denies them.

59. Micron admits that paragraph 59 cites to Exhibit 9 of the Complaint, which states in part "[i]ncluding a different power delivery solution on the DIMM and adding a command/address (CA) bus definition have freed up additional pins for isolation enhancements." Micron denies the remainder of paragraph 59 to the extent that it does not accurately quote this document and any remaining allegation.

High Bandwidth Memory ("HBM")

60. Micron admits that HBM is a type of memory technology. Micron denies that the remaining allegations in paragraph 60 of the Complaint are complete or accurate, and on that basis denies them.

61. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the image shown in paragraph 61 of the Complaint. Except as expressly admitted, Micron denies the

remaining allegations of paragraph 61.

62. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the language "[h]igh-bandwidth memory (HBM) is the fastest DRAM on the planet, designed for applications that demand the maximum bandwidth between memory and processing," "[b]y tightly integrating through-silicon-via (TSV) stacked memory die with the host application-specific integrated circuit (ASIC) . . ., in the same chip package, Micron delivers the best bandwidth possible," and "HBM2E device provides top energy efficiency and high capacity in a very small footprint." Micron denies that the remaining allegations in paragraph 62 of the Complaint are complete or accurate, and on that basis denies them.

63. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the images shown in paragraph 63 of the Complaint. Micron denies that the remaining allegations in paragraph 63 of the Complaint are complete or accurate, and on that basis denies them.

64. Micron admits that the Complaint purports to define the "Accused HBM Products" as stated in paragraph 64. Except as expressly admitted, Micron denies the remaining allegations of paragraph 64.

65. Micron admits that the Complaint purports to define the "Accused HBM Products" as stated in paragraph 65. Except as expressly admitted, Micron denies the remaining allegations of paragraph 65.

FIRST CLAIM FOR RELIEF – '506 PATENT

66. Micron repeats and incorporates by reference its responses to the allegations of the foregoing paragraphs of the Complaint as described above.

67. Micron denies the allegations of paragraph 67.

68. Micron admits that a purported copy of a Micron DDR4 SDRAM LRDIMM Core product description document is attached to the Complaint as Exhibit 16. Micron denies the remainder of paragraph 68 to the extent that it does not accurately quote this document and any remaining allegation.

69. Micron admits that a purported copy of a Micron DDR4 SDRAM LRDIMM Core product description document is attached to the Complaint as Exhibit 16, and that Exhibit 16 includes the images shown in paragraph 69 (pg. 29) of the Complaint and the language "[t]o reduce the electrical load on the host memory controller's command, address, and control bus." Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 69 (pg. 30) of the Complaint. Micron denies the remainder of paragraph 69 to the extent that it does not accurately quote the documents referenced in paragraph 69 and any remaining allegation.

70. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 70 of the Complaint. Micron denies the remainder of paragraph 70 to the extent that it does not accurately quote this document and any remaining allegation.

71. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 71 of the Complaint. Micron denies the remainder of paragraph 71 to the extent that it does not accurately quote this document and any remaining allegation.

72. Micron admits that the image included in paragraph 72 appears to have been taken from JEDEC Standard No. JESD82-32A (August 2019) that is attached to the Complaint as Exhibit 18. Micron denies the remainder of paragraph 72 to the extent that it does not accurately quote

the documents referenced in paragraph 72 and any remaining allegation.

73. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 73 of the Complaint. Micron denies the remainder of paragraph 73 to the extent that it does not accurately quote this document and any remaining allegation.

74. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 74 of the Complaint. Micron denies the remainder of paragraph 74 to the extent that it does not accurately quote this document and any remaining allegation.

75. Micron denies the allegations of paragraph 75.

76. Micron denies the allegations of paragraph 76.

77. Micron denies the allegations of paragraph 77.

SECOND CLAIM FOR RELIEF – '339 PATENT

78. Micron repeats and incorporates by reference its responses to the allegations of the foregoing paragraphs of the Complaint as described above.

79. Micron denies the allegations of paragraph 79.

80. Micron admits that a purported copy of a Micron DDR4 SDRAM LRDIMM Core product description document is attached to the Complaint as Exhibit 16, and that Exhibit 16 includes the images shown in paragraph 80 (pg. 38) of the Complaint and the language "[t]o reduce the electrical load on the host memory controller's command, address, and control bus." Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 80 (pg. 39) of the Complaint. Micron denies the remainder of paragraph 80 to the extent that it does not accurately quote the documents referenced in paragraph 80 and any remaining allegation.

81. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 81 of the Complaint. Micron denies the remainder of paragraph 81 to the extent that it does not accurately quote this document and any remaining allegation.

82. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 82 of the Complaint. Micron denies the remainder of paragraph 82 to the extent that it does not accurately quote this document and any remaining allegation.

83. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image referenced in paragraph 83 of the Complaint. Micron denies the remainder of paragraph 83 to the extent that it does not accurately quote this document and any remaining allegation.

84. Micron admits that a purported copy of a Micron MTA36ASF4G72LZ datasheet is attached to the Complaint as Exhibit 15 and includes the image shown in paragraph 84 of the Complaint. Micron denies the remainder of paragraph 84 to the extent that it does not accurately quote this document and any remaining allegation.

85. Micron admits that the image included in paragraph 85 appears to have been taken from JEDEC Standard No. JESD79-4C (January 2020) that is attached to the Complaint as Exhibit 19. Micron denies the remainder of paragraph 85 to the extent that it does not accurately quote the documents referenced in paragraph 85 and any remaining allegation.

86. Micron admits that the image included in paragraph 86 appears to have been taken from JEDEC Standard No. 21C (4.20.27) that is attached to the Complaint as Exhibit 20. Micron denies the remainder of paragraph 86 to the extent that it does not accurately quote this document

and any remaining allegation.

87. Micron admits that the image included in paragraph 87 appears to have been taken from JEDEC Standard No. JESD82-32A (August 2019) that is attached to the Complaint as Exhibit 18. Micron denies the remainder of paragraph 87 to the extent that it does not accurately quote the documents referenced in paragraph 87 and any remaining allegation.

88. Micron admits that the images included in paragraph 88 appear to have been taken from JEDEC Standard No. JESD82-32A (August 2019) that is attached to the Complaint as Exhibit 18. Micron denies the remainder of paragraph 88 to the extent that it does not accurately quote the documents referenced in paragraph 88 and any remaining allegation.

89. Micron denies the allegations of paragraph 89.

90. Micron denies the allegations of paragraph 90.

91. Micron denies the allegations of paragraph 91.

THIRD CLAIM FOR RELIEF – '918 PATENT

92. Micron repeats and incorporates by reference its responses to the allegations of the foregoing paragraphs of the Complaint as described above.

93. Micron denies the allegations of paragraph 93.

94. Micron admits that paragraph appears to include an annotated image from the Complaint's Exhibit 14. Micron denies the remainder of paragraph 94 to the extent that it does not accurately quote this document and any remaining allegation.

95. Micron admits that a purported copy of a Micron Technical Brief titled "Micron® DDR5: Key Module Features" is attached to the Complaint as Exhibit 8, and that Exhibit 8 includes the image shown in paragraph 95 of the Complaint and the language "DDR5 modules introduce local voltage regulation on the module. The voltage regulation is achieved by a power management integrated circuit (PMIC). The PMIC provides the brains of a smart voltage regulation system for

the DDR5 DIMM, enabling configurability of voltage ramps and levels as well as current monitoring. Power management has historically been done on the motherboard. The introduction of PMICs allows additional features like threshold protection, error injection capabilities, programmable power on sequence, and power management features. The presence of the PMIC on the module enables better power regulation and reduces complexity of the motherboard design by reducing the scope of DRAM power delivery (PDN) management." Micron denies the remainder of paragraph 95 to the extent that it does not accurately quote the documents referenced in paragraph 95 and any remaining allegation.

96. Micron admits that the images included in paragraph 96 that are annotated by Netlist appear to have been taken from JEDEC Standard No. JESD301-1 (June 2020) that is attached to the Complaint as Exhibit 21. Micron denies the remainder of paragraph 96 to the extent that it does not accurately quote this document and any remaining allegation.

97. Micron admits that a purported copy of a Micron Technical Brief titled "Micron® DDR5: Key Module Features" is attached to the Complaint as Exhibit 8 and includes the image shown at the bottom of page 53 in paragraph 97 of the Complaint. Micron admits that the two top images included on page 54 in paragraph 97 appear to have been taken from JEDEC Standard No. JESD79-5 (July 2020) that is attached to the Complaint as Exhibit 22. Micron admits that the bottom image included on page 54 in paragraph 97 appears to have been taken from JEDEC Standard No. JESD82-511 (August 2021) that is attached to the Complaint as Exhibit 17. Micron denies the remainder of paragraph 97 to the extent that it does not accurately quote the documents referenced in paragraph 97 and any remaining allegation.

98. Micron admits that the image included in paragraph 98 appears to have been taken from JEDEC Standard No. JESD82-511 (August 2021) that is attached to the Complaint as Exhibit

17. Micron denies the remainder of paragraph 98 to the extent that it does not accurately quote this document and any remaining allegation.

99. Micron admits that the image included in paragraph 99 appears to have been taken from JEDEC Standard No. JESD82-511 (August 2021) that is attached to the Complaint as Exhibit 17. Micron denies the remainder of paragraph 99 to the extent that it does not accurately quote this document and any remaining allegation.

100. Micron admits that Netlist alleged infringement of the '918 Patent in the Complaint. Micron denies the remaining allegations in paragraph 100 of the Complaint.

FOURTH CLAIM FOR RELIEF – '054 PATENT

101. Micron repeats and incorporates by reference its responses to the allegations of the foregoing paragraphs of the Complaint as described above.

102. Micron denies the allegations of paragraph 102.

103. Micron admits that a purported copy of a Micron White Paper titled "Micron® DDR5: Client Module Features" is attached to the Complaint as Exhibit 10 and includes the image shown in paragraph 103 of the Complaint. Micron denies the remainder of paragraph 103 to the extent that it does not accurately quote this document and any remaining allegation.

104. Micron admits that a purported copy of a Micron White Paper titled "Micron® DDR5: Client Module Features" is attached to the Complaint as Exhibit 10 and includes the images shown on page 57 in paragraph 104 of the Complaint. Micron admits that a purported copy of a Micron product description document titled "DDR5 SDRAM UDIMM Core" is attached to the Complaint as Exhibit 13 and includes the image shown on page 57 in paragraph 104 of the Complaint. Micron denies the remainder of paragraph 104 to the extent that it does not accurately quote the documents referenced in paragraph 104 and any remaining allegation.

105. Micron admits that a purported copy of a Micron Technical Brief titled "Micron®

DDR5: Key Module Features" is attached to the Complaint as Exhibit 8 and includes the language "[t]he PMIC provides the brains of a smart voltage regulation system for the DDR5 DIMM, enabling configurability of voltage ramps and levels as well as current monitoring." Micron denies the remainder of paragraph 105 to the extent that it does not accurately quote the documents referenced in paragraph 105 and any remaining allegation.

106. Micron admits that the accused DDR5 products include components. Micron denies that the allegations in paragraph 106 of the Complaint are complete or accurate, and on that basis denies them.

107. Micron admits that the images included in paragraph 107 appear to have been taken from JEDEC Standard No. JESD301-1 (June 2020) that is attached to the Complaint as Exhibit 21. Micron denies the remainder of paragraph 107 to the extent that it does not accurately quote this document and any remaining allegation.

108. Micron admits that the images included in paragraph 108 appear to have been taken from JEDEC Standard No. JESD301-1 (June 2020) that is attached to the Complaint as Exhibit 21. Micron denies the remainder of paragraph 108 to the extent that it does not accurately quote this document and any remaining allegation.

109. Micron denies the allegations of paragraph 109.

FIFTH CLAIM FOR RELIEF – '060 PATENT

110. Micron repeats and incorporates by reference its responses to the allegations of the foregoing paragraphs of the Complaint as described above.

111. Micron denies the allegations of paragraph 111.

112. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the images shown in paragraph 112 of the Complaint. Micron denies the remainder of paragraph 112 to the

extent that it does not accurately quote this document and any remaining allegation.

113. Micron denies that the allegations in paragraph 113 of the Complaint are complete or accurate, and on that basis denies them.

114. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the language "[t]he HBM2E DRAM is soldered to a silicon interposer that routes all interface signals in very tiny traces to the host ASIC." Micron admits that a purported copy of a Micron White Paper titled "The Demand for High-Performance Memory" is attached to the Complaint as Exhibit 11 and includes the image shown in paragraph 114 of the Complaint. Micron denies the remainder of paragraph 114 to the extent that it does not accurately quote the documents referenced in paragraph 114 and any remaining allegation.

115. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the images shown in paragraph 115 of the Complaint. Micron denies the remainder of paragraph 115 to the extent that it does not accurately quote the documents referenced in paragraph 115 and any remaining allegation.

116. Micron denies that the allegations in paragraph 116 of the Complaint are complete or accurate, and on that basis denies them.

117. Micron denies that the allegations in paragraph 117 of the Complaint are complete or accurate, and on that basis denies them.

118. Micron denies the allegations of paragraph 118.

SIXTH CLAIM FOR RELIEF – '160 PATENT

119. Micron repeats and incorporates by reference its responses to the allegations of the foregoing paragraphs of the Complaint as described above.

120. Micron denies the allegations of paragraph 120.

121. Micron admits that paragraph 121 appears to refer to Exhibit 12 to the Complaint. Micron denies the remainder of paragraph 121 to the extent that it does not accurately quote this document and any remaining allegation.

122. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the images shown in paragraph 122 of the Complaint. Micron denies the remainder of paragraph 122 to the extent that it does not accurately quote this document and any remaining allegation.

123. Micron denies that the allegations in paragraph 123 of the Complaint are complete or accurate, and on that basis denies them.

124. Micron admits that a purported copy of a Micron Technical Brief titled "Integrating and Operating HBM2E Memory" is attached to the Complaint as Exhibit 9 and includes the language "[t]he HBM2E interfaces use regular pull/push drivers with programmable driver strength for signaling." Micron denies the remainder of paragraph 124 to the extent that it does not accurately quote this document and any remaining allegation.

125. Micron denies the allegations of paragraph 125.

DEMAND FOR JURY TRIAL

126. Micron admits that the Complaint purports to demand a trial by jury on all issues so triable.

[NETLIST'S] PRAYER FOR RELIEF

Micron denies that Netlist is entitled to any relief in this action, as requested in paragraphs (A) through (H) of Netlist's Prayer for Relief or otherwise.

MICRON'S AFFIRMATIVE DEFENSES

Subject to its responses above, and upon information and belief, Micron alleges and asserts these defenses in response to the allegations in the Complaint, undertaking the burden of proof only as to those defenses deemed affirmative defenses by law, regardless of how such defenses are denominated. In addition to the affirmative defenses described below, subject to the responses above, Micron reserves all rights to allege additional defenses pursuant to any scheduling order that become known through the course of discovery or otherwise.

FIRST AFFIRMATIVE DEFENSE – FAILURE TO STATE A CLAIM

1. Netlist has failed to plead its claims with sufficient specificity or factual support to place Micron on notice of the claims Netlist is asserting against it, such that Netlist has failed to state a claim upon which relief can be granted.

SECOND AFFIRMATIVE DEFENSE – NON-INFRINGEMENT

2. Micron has not infringed and does not infringe (i) directly, either literally or under the doctrine of equivalents, (ii) indirectly by contributing to infringement by others, either literally or under the doctrine of equivalents, and/or (iii) indirectly by inducing others to infringe, either literally or under the doctrine of equivalents, any valid and enforceable claim of the Asserted Patents, willfully or otherwise.

THIRD AFFIRMATIVE DEFENSE – INVALIDITY

3. One or more claims of the Asserted Patents are invalid for failure to meet the conditions of patentability and/or otherwise comply with the requirements of 35 U.S.C. §§ 101 *et seq*., including, but not limited to, 35 U.S.C. §§ 101, 102, 103, and/or 112.

FOURTH AFFIRMATIVE DEFENSE – PROSECUTION HISTORY ESTOPPEL

4. One or more claims are limited by the text of the Asserted Patents and prosecution histories of the Asserted Patents and related patents such that Netlist is estopped, or otherwise precluded, from asserting that the claim is infringed by Micron, literally or by equivalents.

FIFTH AFFIRMATIVE DEFENSE – WAIVER AND ESTOPPEL

5. Netlist's claims for relief, in whole or in part, are barred by the doctrines of waiver and/or equitable estoppel.

SIXTH AFFIRMATIVE DEFENSE – LICENSE AND COVENANT NOT TO SUE

6. Netlist's claims for relief, in whole or in part, are precluded to the extent any of the claims of the Asserted Patents are subject to a license and covenant not to sue, express and/or implied.

SEVENTH AFFIRMATIVE DEFENSE – STATUTE OF LIMITATIONS

7. Netlist's recovery for any infringement of the Asserted Patents that it might establish is limited to any established infringement occurring no more than six years before the filing of this lawsuit, pursuant to 35 U.S.C. § 286.

EIGHTH AFFIRMATIVE DEFENSE – LACK OF MARKING

8. Netlist's recovery for alleged infringement of the Asserted Patents, if any, is limited to alleged infringement committed after Netlist provided actual or constructive notice of infringement under 35 U.S.C. § 287.

NINTH AFFIRMATIVE DEFENSE – NO WILLFUL INFRINGEMENT

9. Netlist fails to state a claim for relief against Micron for enhanced or increased damages for willful infringement.

TENTH AFFIRMATIVE DEFENSE – NO EXCEPTIONAL CASE

10. Netlist fails to state a claim for relief against Micron for exceptional case under 35 U.S.C. § 285.

ELEVENTH AFFIRMATIVE DEFENSE – NO COSTS

11. Netlist is barred by 35 U.S.C. § 288 from recovering any costs associated with this lawsuit.

TWELFTH AFFIRMATIVE DEFENSE – LACK OF STANDING

12. To the extent that Netlist was not the sole and total owner of all substantial rights in any of the Asserted Patents as of the filing date of the Complaint, Netlist lacks standing to bring one or more claims in this lawsuit.

THIRTEENTH AFFIRMATIVE DEFENSE – EXHAUSTION

13. Netlist's claims are barred, in whole or in part, by the doctrine of patent exhaustion.

FOURTEENTH AFFIRMATIVE DEFENSE – ABSENCE OF DAMAGES

14. Netlist has not suffered and will not suffer any injury or damages as a result of Micron's alleged conduct.

FIFTEENTH AFFIRMATIVE DEFENSE – LACHES, INEQUITABLE CONDUCT, AND UNCLEAN HANDS

15. Netlist is barred, in whole or in part, under principles of equity, including laches, prosecution laches, inequitable conduct, and/or unclean hands. Netlist is also barred by issue preclusion from reasserting or altering its positions on factual and legal issues that were previously adjudicated.

16. Individuals substantively involved in the prosecution of the '506 Patent knew about material and non-cumulative prior art by virtue of their participation in JEDEC standards meetings. On information and belief, these individuals specifically intended to deceive the Patent Office into believing that the claims of the '506 Patent were patentable by withholding the relevant art from the examiner during prosecution of the patent.

A. Background on the Alleged Invention, the Prosecution of the '506 Patent, and Events Occurring During the Same

17. The '506 Patent issued from a series of continuation applications: U.S. Patent Application Nos. 15/820,076 (U.S. Patent No. 10,268,608); 15/426,064 (U.S. Patent No. 9,824,035); 14/846,993 (U.S. Patent No. 9,563,587); and 13/952,599 (U.S. Patent No. 9,128,632).

This chain of continuation applications ultimately claims priority to U.S. Provisional Patent Application No. 61/676,883, which was filed on July 27, 2012. All the applications name Hyun Lee and Jayesh R. Bhakta as the inventors.

18. The '506 Patent incorporates by reference a number of Netlist's other patent applications, including U.S. Patent Application Nos. 14/715,486 (U.S. Patent No. 9,858,821); 13/970,606 (U.S. Patent No. 9,606,907); 12/504,131 (U.S. Patent No. 8,417,870); 12/761,179 (U.S. Patent No. 8,516,185); 13/287,042 (U.S. Patent No. 8,756,364); and 13/287,081 (U.S. Patent No. 8,516,188).

19. Netlist filed a terminal disclaimer for the '506 Patent on April 10, 2020, over the '608, '035, '587, and '632 patents.

1. Hyun Lee's and Jayesh Bhakta's Alleged Conception and Reduction to Practice, and Regular Attendance at JEDEC Meetings

20. Hyun Lee continued to regularly attend JEDEC meetings for at least the JC-40 committee and the JC-45 committee in 2011 and 2012, as well as before and after that time frame. For instance, on information and belief, Hyun Lee attended at least the following JC-40 meetings: No. 168, Dec. 8, 2011; No. 169, Mar. 5, 2012; and No. 170, June 4, 2012. And, on information and belief, Hyun Lee attended at least the following JC-45 meetings: No. 33, Dec. 7-8, 2011; No. 34, Mar. 5, 2012; and No. 35, June 4, 2012.

21. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those committees, including JESD82-32, dated November 2016, as well as prior drafts of it. For example, Intel presented and discussed Committee Item Number 158.01 ("DDR4 LRDIMM Proposal") at the December 8, 2011 meeting of JC-40, Committee Item Number 0311.14 ("Proposed DDR4 DB Training Modes") at the March

25, 2012 meeting of JC-40, and Committee Item Number 0311.12 ("Proposed DDR DB Buffer Control Words") at the June 4, 2012 meeting of JC-40.

22. On information and belief, the JESD82-32 standard was circulated at or before, and discussed at and voted on at or before, the JC-40 and JC-45 committee meetings that Hyun Lee attended.

23. On information and belief, draft Committee Item Number 158.01 was created by employees of Intel Corp. and circulated at or before, and discussed at, the JC-40 committee meeting on December 8, 2011 that Hyun Lee attended.

24. On information and belief, draft Committee Item Number 0311.14 was created by employees of Intel Corp. and circulated at or before, and discussed at, the JC-40 committee meeting on Mar. 5, 2012 that Hyun Lee attended.

25. On information and belief, draft Committee Item Number 0311.12 was created by employees of Intel Corp. and circulated at or before, and discussed at, the JC-40 committee meeting on June 4, 2012 that Hyun Lee attended.

26. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those subcommittees.

27. Draft specifications, ballots, and presentations distributed to the members of the JC-40 and/or JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. As such, they are prior art under 35 U.S.C. § 102 at least as of those distribution dates.

28. Distributed specifications, such as JESD82-32, are prior art under 35 U.S.C. § 102

at least as of their release dates.

29. The provisional application to which the '506 Patent claims priority was filed on July 12, 2012, naming Hyun Lee as the inventor. Jayesh R. Bhakta was named as a co-inventor after the provisional was filed.

30. On information and belief, and based on Netlist's apparent view of the scope of the alleged invention, each of the draft DDR4 LRDIMM drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '506 Patent.

31. On information and belief, after attending the June 4, 2012 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist and hurriedly completed drafting the provisional application to which the '506 Patent claims priority, naming himself as the inventor, and had a provisional application filed on July 27, 2012. Netlist filed a request to correct inventorship on September 26, 2012, adding Jay R. Bhakta as a co-inventor.

2. '506 Patent Prosecution and Corresponding Events

32. Netlist filed the application, No. 16/391,151, that issued as the '506 Patent on April 22, 2019.

33. On August 20, 2019, Netlist filed an Information Disclosure Statement (IDS) Form containing seven sheets. JEDEC DDR LRDIMM drafts and specifications were not included.

34. On January 8, 2020, Netlist filed an Information Disclosure Statement (IDS) Form containing twenty-two sheets. The cited references include numerous entire prosecution histories for other Netlist applications. JEDEC DDR LRDIMM drafts and specifications were not included.

35. On January 10, 2020, the examiner issued a Non-Final Rejection rejecting then-pending claim 1 for obviousness-type double patenting and as anticipated by U.S. Patent No. 8,565,033 ("Manoharajah").

36. On April 10, 2020, Netlist filed an Amendment and Request for Reconsideration

after Non-Final Rejection. Netlist's response included a Terminal Disclaimer and canceled claim 1. Netlist added claims 2–21.

37. On July 23, 2020, the examiner issued a Notice of Allowance for the application that issued as the '506 Patent.

38. On October 16, 2020, Netlist filed an Amendment after Allowance, and on October 22, 2020, Netlist paid the issue fee for the application that issued as the '506 Patent.

39. On November 11, 2020, the examiner accepted the Amendment.

40. On November 18, 2020, the examiner issued an issue date notification for the application that issued as the '506 Patent. That notification specified an issue date of December 8, 2020.

41. Netlist took no action to withdraw the application that issued as the '506 Patent from issuance, or to otherwise continue prosecution of that application, and the application issued as the '506 Patent on December 8, 2020.

B. Netlist's Failure to Disclose the Drafts and Presentations for DDR4 LRDIMMs from the Dec. 8, 2011, Mar. 5, 2012, and June 4, 2012 JEDEC JC-40 Meetings Attended by Hyun Lee, and False Portrayal of Hyun Lee and Jayesh R. Bhakta as Inventors.

42. At least according to Netlist's characterizations of the inventive aspects of the disclosure and claims of the '506 Patent, the draft specifications and related presentations for DDR4 LRDIMMs that were presented at the Dec. 8, 2011, Mar. 5, 2012, and June 4, 2012 meetings disclose the key allegedly inventive aspects of the claims of the '506 Patent. These draft specifications and presentations include Committee Item Number 158.01 from the December 2011 meeting, Committee Item Number 0311.14 from the March 2012 meeting, and Committee Item Number 0311.12 from the June 2012 meeting.

43. Even though at least Hyun Lee was present at the JEDEC meeting at which those

presentations were made, witnessed those presentations, and was present for the discussions that occurred about them, and immediately thereafter drafted the provisional application to which the '506 Patent claims priority, on information and belief, Hyun Lee did not disclose any of these drafts and the presentations to the examiner of the application that issued as the '506 Patent.

44. Those drafts and presentations are prior art under 35 U.S.C. § 102 at least as of the meeting in which they were presented and discussed, and are not cumulative of other art or information before the examiner of the application that issued as the '506 Patent.

45. Those drafts and presentations also illustrate that Hyun Lee falsely portrayed himself and Jayesh R. Bhakta as the inventors of the alleged inventions claimed in the '506 Patent. At a minimum, those drafts and presentations illustrate that Hyun Lee, based on Netlist's infringement allegations, derived at least portions of the allegedly inventive aspects of the claimed inventions from others in attendance at the JC-40 meetings, who made those presentations on behalf of Intel, among others.

46. The Patent Office would not have allowed at least one claim of the '506 Patent to issue had it been aware of those drafts and presentations, at least because it would have found the claims obvious over those drafts and presentations (either in combination with the knowledge of one of ordinary skill or in combination with art disclosing the basic architecture and functionality of DDR4 LRDIMMs), that there are joint inventors that were not properly named on the applications that issued as the '506 Patent, and/or that the alleged inventions claimed therein had been derived in whole or in part from another.

47. The drafts and presentations that Hyun Lee failed to disclose to the Patent Office were not cumulative of other art before the examiner. The examiner stated that he allowed the

claims because the art of record did not teach or suggest:

> a memory controller system with memory modules having control and address signal lines implemented to be used corresponding to memory read operations to and from memory devices of the memory module that are arranged in multiple ranks with data buffers couple to memory devices, where memory read operations output read data and read strobes associated with memory read operations, and where the data buffer implemented delaying of a first read strobe by a predetermined amount, i.e. generating a delayed read strobe, sampling the first section of read data using the delayed read strobe, and transmitting the section of read data to a data bus, where the predetermined amount of delay is based at least on signals received by the data buffer [during one or more previous operations] as claimed.

Notice of Allowability at 3–4. The withheld drafts and presentations for DDR4 LRDIMM explained the structure and operation of DDR4 LRDIMM devices, which Netlist argues practice the claims of the '506 Patent. For example, Committee Item Number 158.01 shows the accused DDR4 LRDIMM's structure, which Netlist argues includes the claimed "memory devices of the memory module that are arranged in multiple ranks with data buffers couple to memory device." Committee Item No. 158.01 at 2. Moreover, the draft specifications explain DDR LRDIMM's training modes including "Read Delay Training." *See, e.g.*, Committee Item No. 311.14 at 8–9. Netlist argues that these training modes are used to determine the claimed "predetermined amount."

48. On information and belief, Hyun Lee specifically intended to deceive the Patent Office into believing that Hyun Lee and Jayesh R. Bhakta were the sole inventors of the '506 Patent, and/or that the claims of those patents are otherwise patentable, by withholding those drafts and presentations from the patent examiner during prosecution of the application that issued as the '506 Patent. On information and belief, Hyun Lee engaged in this conduct as part of a scheme to

monetize Netlist's patents through litigation against the industry.

* * * *

49. Inequitable Conduct: Any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist committed inequitable conduct during the prosecution of the '506 Patent that renders the '506 Patent unenforceable.

50. Unclean Hands: Furthermore, any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist has unclean hands in relation to its assertion of the '506 Patent that renders the '506 Patent unenforceable.

SIXTEENTH AFFIRMATIVE DEFENSE – 28 U.S.C. § 1498

51. Netlist's recovery for alleged infringement of the Asserted Patents, if any, is limited pursuant to 28 U.S.C. § 1498 to the extent that any alleged infringement, in whole or part, is attributable to the United States government.

SEVENTEENTH AFFIRMATIVE DEFENSE – BREACH OF RAND LICENSING OBLIGATION

52. Netlist's claims for injunctive relief are barred, in whole or in part, because of its failure to offer Micron a license to various of the Asserted Patents on reasonable terms and conditions that are demonstrably free of unfair discrimination (i.e., "RAND terms").

53. Netlist is presently a member of JEDEC. Netlist committed various of the Asserted Patents to various JEDEC standards pursuant to the JEDEC Patent Policy, which sets certain obligations for owners of patents (like the Asserted Patents) that it reasonably believes are essential to one or more JEDEC standards. The JEDEC Patent Policy, as set forth in the JEDEC Manual of Organization and Procedure, states in relevant part that "[a] license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination . . .."

54. Netlist has asserted that various of the Asserted Patents must be practiced to implement standards relating to memory technologies promulgated by the leading standard-setting organization in the memory technology field, JEDEC. Netlist therefore asserts that various of the Asserted Patents are "essential" to the implementation of the JEDEC standards in question (such allegedly standard "essential" patents are referred to herein as "SEPs"). JEDEC's semiconductor memory standards enable interoperability—that is, the ability of memory products made by different manufacturers to work together and with computer and electronic devices made by others. JEDEC standards are widely implemented and, for many types of semiconductor memory products, it is imperative that they comply with JEDEC standards in order to be commercially viable.

55. Netlist has participated in the development of standards relating to memory technologies in JEDEC. Pursuant to JEDEC's Patent Policy, Netlist submitted a "License Assurance/Disclosure Form" applicable to various of the Asserted Patents pursuant to which it has (a) disclosed each of those patents, or patents claiming priority to the same filing as various of the Asserted Patents, to be potentially essential to certain JEDEC standards and (b) committed to offer to license any claim of various of the Asserted Patents that is essential to the implementation of relevant JEDEC standards to those wishing to implement those JEDEC standards on RAND terms.

56. Moreover, pursuant to the JEDEC Patent Policy, which is binding upon Netlist, simply by virtue of its membership on the committees that developed the standards to which Netlist asserts the claims of various of the Asserted Patents are essential, Netlist is obligated to offer to license those claims to all potential licensees like Micron on RAND terms.

57. Netlist has breached its obligations to offer to license various of the Asserted Patents on RAND terms by, among other things: (a) failing to offer to license its SEPs to Micron

on terms that are reasonable and (b) seeking injunctive relief against Micron based upon its alleged infringement of various of the Asserted Patents despite Micron's willingness to engage in discussions about licensing any claim shown to be valid and infringed on RAND terms. To date, and despite Micron's attempts to obtain such a showing, Netlist has failed to show that any asserted claim is valid and infringed.

RESERVATION OF ADDITIONAL AFFIRMATIVE DEFENSES

Micron reserves all affirmative defenses under Rule 8(c) of the Federal Rules of Civil Procedure, the Patent Laws of the United States, and any other defenses at law or in equity that may exist now or that may be available in the future based on discovery and further factual investigation in this action.

Dated: August 4, 2022

Respectfully submitted,

By: */s/ Natalie Arbaugh*

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ATTORNEYS FOR MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS LLC

CERTIFICATE OF SERVICE

I hereby certify that on August 4, 2022, the foregoing document was electronically filed with the Clerk of the Court using the Court's CM/ECF system, which will send notification of such filing to all counsel of record, including counsel for Plaintiff, Netlist, Inc.

/s/ Natalie Arbaugh
Natalie Arbaugh